

CLAIMS

We Claim:

1. A random access memory of magnetic elements comprising:

an array of bit cells;

5 an array of write conductors for use in writing to a selected bit cell of said array of bit cells, wherein a write current applied to a write conductor of a selected bit cell is subject to producing a magnetic field about the corresponding write conductor, the magnetic field including a stray portion thereof subject to disturbing a non-selected  
10 bit cell of a neighboring write conductor; and

a plurality of write drivers coupled to first ends of corresponding ones of the plurality of write conductors, wherein at least one write driver is configured as follows: (a) for switching a write current onto a  
15 corresponding write conductor in response to selection of a bit cell of the corresponding write conductor; and (b) for switching a disturb counteracting current onto the corresponding write conductor in response to non-selection of a bit cell associated with the corresponding write conductor, the disturb counteracting current including a recycled portion of the write current of a neighboring  
20 write conductor of a selected bit cell.

2. The random access memory of claim 1, wherein the disturb counteracting current produces a second magnetic field about the corresponding write conductor.

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3. The random access memory of claim 2, further wherein the second magnetic field is adapted to counteract an effect on a non-selected bit cell of the corresponding write conductor due to a stray portion of a magnetic field of a neighboring write conductor of a selected bit cell.

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4. The random access memory of claim 3, still further wherein the second magnetic field is oriented in a direction opposite to that of the magnetic field of the neighboring write conductor of the selected bit cell.

10 5. The random access memory of claim 1, wherein the disturb counteracting current is a reverse current of a portion of the write current.

6. The random access memory of claim 5, further wherein the disturb counteracting current does not in itself lead to disturbing of bit cells of other  
15 neighboring write conductors.

7. The random access memory of claim 1, wherein switching the disturb counteracting current includes selectively switching the disturb counteracting current onto the corresponding write conductor.

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8. The random access memory of claim 1, wherein the recycled portion of the write current is substantially equally divided among the plurality of write conductors minus one.

25 9. The random access memory of claim 1, further comprising:

a current redistribution bus coupled to second ends of corresponding ones of the plurality of the write conductors, said current redistribution bus for redistributing the write current of a first write conductor into at least one disturb counteracting current to be distributed among at least one of the plurality of  
5 write conductors other than the first write conductor.

10. The random access memory of claim 9, wherein redistributing the write current further includes redistributing the same as a function of a proximity to the first write conductor.

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11. The random access memory of claim 9, wherein redistributing among at least one of the plurality of write conductors other than the first write conductor is further a function of a desired counteracting effect on the stray portion of the magnetic field.

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12. The random access memory of claim 9, wherein the redistribution is still further a function of at least one selected from the group consisting of immediately adjacent write conductors of non-selected bit cells alone, even numbered ones of adjacent write conductors of non-selected bit cells, and odd  
20 numbered ones of adjacent write conductors of non-selected bit cells.

13. The random access memory of claim 1, wherein the at least one write driver further includes a first switch and a second switch, the first switch for switching the write current onto the corresponding write conductor in response  
25 to the selection of the bit cell of the corresponding write conductor, and the second switch for coupling the disturb counteracting current to a same

corresponding write conductor in response to non-selection of a bit cell associated with the corresponding write conductor.

14. The random access memory of claim 13, further wherein a state of the first switch is mutually exclusive of a state of the second switch.

15. The random access memory of claim 13, further wherein a state of the first switch is normally ON, and still further wherein responsive to selection of a bit cell on a respective write conductor, the first switch turns OFF and the second switch turns ON.

16. The random access memory of claim 1, wherein the write current of the write conductor of the selected bit cell is divided between a subset of write conductors of non-selected bit cells.

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17. The random access memory of claim 13, further wherein the first switch includes a current controlled switch that comprises of a NAND gate coupled to an input of a current mirror, still further wherein the first switch couples a first power supply voltage to a corresponding write conductor.

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18. The random access memory of claim 17, further wherein the second switch includes an inverter coupled to a p-type transistor, still further wherein the second switch couples a second voltage power supply to the corresponding write conductor.

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19. The random access memory of claim 18, wherein the first power supply voltage corresponds to a lower voltage potential bus  $V_{SS}$  and the second power supply voltage corresponds to a higher voltage potential bus  $V_{DD}$ .

5 20. The random access memory of claim 1, wherein the bit cells include magnetoresistive memory cells.

21. A method of reducing write field disturb in a random access memory of magnetic elements, the random access memory including an array of bit cells,  
10 an array of write conductors for use in writing to a selected bit cell of the array of bit cells, wherein a write current applied to a write conductor of a selected bit cell is subject to producing a magnetic field about a corresponding write conductor, the magnetic field including a stray portion thereof subject to disturbing a non-selected bit cell of a neighboring write conductor, and a  
15 plurality of write drivers, said method comprising:

coupling the plurality of write drivers to first ends of corresponding ones of the plurality of write conductors; and

configuring at least one write driver for: (a) switching a write current onto a corresponding write conductor in response to selection of a bit cell of the  
20 corresponding write conductor and (b) switching a disturb counteracting current onto the corresponding write conductor in response to non-selection of a bit cell associated with the corresponding write conductor, wherein switching the disturb counteracting current includes recycling a portion of the write current of a neighboring write conductor of a selected bit cell.

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22. The method of claim 21, further comprising:

producing a second magnetic field about the corresponding write conductor in response to the disturb counteracting current.

23. The method of claim 22, further comprising:

5        adapting the second magnetic field to counteract an effect on a non-selected bit cell of the corresponding write conductor due to a stray portion of a magnetic field of a neighboring write conductor of a selected bit cell.

24. The method of claim 21, wherein the disturb counteracting current is a  
10        reverse current of a portion of the write current.

25. The method of claim 21, wherein switching the disturb counteracting current includes selectively switching the disturb counteracting current onto the corresponding write conductor.

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26. The method of claim 21, further comprising:

      substantially equally dividing a recycled portion of the write current among the plurality of write conductors minus one.

20    27. The method of claim 21, further comprising:

      coupling a current redistribution bus to second ends of corresponding ones of the plurality of the write conductors, the current redistribution bus for redistributing the write current of a first write conductor into at least one disturb counteracting current to be distributed among at least one of the plurality of  
25    write conductors other than the first write conductor.

28. The method of claim 27, wherein redistributing the write current further includes redistributing the same as a function of a proximity to the first write conductor.

5 29. The method of claim 27, wherein redistributing among at least one of the plurality of write conductors other than the first write conductor is further a function of a desired counteracting effect on the stray portion of the magnetic field.

10 30. The method of claim 21, further comprising:  
dividing the write current of the write conductor of the selected bit cell between a subset of write conductors of the non-selected bit cells.

15 31. The method of claim 21, wherein the bit cells include magnetoresistive memory cells.